a plurality of metallized bumps in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal.

9. An electronic component according to claim 1, wherein:

the device is a vertical device and the bottom of the device is coupled to the package in the recess.

14. An electronic component comprising:

a package having a recess, the recess including a first deposition-processed conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region and the top terminal is electrically coupled to a second deposition-processed conductive region, and wherein at least a portion of the first and second conductive regions are essentially planar.

34. An electronic component according to claim 32, further comprising:

a metallization layer.

35. An electronic component according to claim 34, wherein:

the metallization layer couples each contact to a redistribution point on the package top, and each contact remains electrically distinct.

In the Specification:

Please replace the paragraph beginning at page 3, line 1, with the following rewritten paragraph:

Fig. 1 is a side view of an electronic component. The electronic component is formed by a silicon package 10 from a silicon wafer surrounding an electronic device 12, preferably a bare die semiconductor device. The silicon package 10 includes a recess 14 in which the electronic device 12 resides. The electronic device 12 in the embodiment shown is a two-terminal device, although other multi-terminal devices, including both vertical and planar devices, may be used. The electronic device shown is a vertical device having a top terminal 15 and a bottom terminal 16. In the recess of the package, a conductive region 17 exists. The conductive region 17 covers all or a portion of the recess 14 and extends to a portion of the top 18 of the silicon package 10. The bottom terminal 16 of the two-terminal electronic device is electrically coupled to the conductive region 17. In preferred embodiments the conductive region is formed from metals such as titanium, copper and chrome. The bottom terminal 16 of the electronic device is secured to the conductive region by a conductive epoxy or solder 19. The recess 14 is filled with dielectric material 20 that surrounds the electronic device 12. If the dielectric layer 20 covers the top terminal 15 of the electronic device 12, the dielectric 20 that resides above the top terminal 15 is removed through photolithography. Dielectric may also be removed at a point where a solder contact for the bottom terminal is desired. A metallization layer 22 is applied over the dielectric after the top terminal 15 of the electronic device 12 is exposed. The metallization is deposited and patterned by standard methods to the desired routing including solder contact areas. In the shown embodiment, another layer of dielectric 25 resides on top of the metallization layer 22 fully encasing the electronic device 12 and only leaving the contacts exposed. It should be understood by those of ordinary skill in the art that for certain electronic devices a second layer of dielectric may not be needed. The solder contacts 21 are then created and preferably reside in the same plane so that the completed electronic component may be easily flip mounted onto a circuit board. In the preferred embodiment, the electronic device is a diode. However, it should be understood to one of ordinary skill in the art that other semiconductor devices, integrated circuits, or other electronic devices may be placed

within the silicon package. This process produces a Wafer Level Chip-Scale Package (WLCSP) using silicon as the package.

Please replace the paragraph beginning at page 7, line 1, with the following rewritten paragraph:

In Fig. 5 is shown a package 510 for a bare die planar electronic device 520 that has all terminals 540 on one side of the chip. In this embodiment, the terminals 540 of the device 520 are repositioned using the technique above. The device 520 is placed into a recess 515 of the package 510 and is adhered to the package using an adhesive 530 to mechanically couple the bare die 520 and the package 510. Into the portion of the recess 515 that is not filled by the bare die is placed a planarizing dielectric material 550. The planarizing material 550 creates an essentially planar surface for applying a layer of metallization 560 so that the terminals 540 of the bare die 520 may be repositioned. Once the terminals 540 are repositioned, a second layer of dielectric 570 is applied keeping only the positions of the final contacts exposed. At the desired position of the final contact a metal contact 580 or soldering bump is added. The electronic component 500 is electrically exposed only at the repositioned contact points 580 with the rest of the electronic device 520 shielded from electrical coupling by the package 510 or dielectric 570. In such a fashion, planar electronic devices having terminals that are positioned too close together and are at such a small scale that the terminals cannot maintain their electrical independence when placed on a circuit board may be made effectively larger by repositioning the contacts on the top of the package. Similarly, the terminals can be repositioned in any configuration that is more convenient for the end user of the electronic components. Thus, utilizing wafer-level processing, a smaller device may be made to be compatible with the dimensional requirements of a circuit board for fabrication of a more complicated product or subassembly.